

REMARKS

Claim Rejections – 35 U.S.C. §112

Claims 2, 10, 19 and 22 are rejected under 35 U.S.C. §112, first paragraph, as failing to comply with the written description requirement. Applicant traverses this rejection.

The examiner alleges that the language “progressive compression” is not supported in the specification. However, compliance with the written description requirement only requires that the meaning of the claims may be ascertainable by reference to the description. *See Lampi Corp. v. American Power Prods., Inc.*, 56 U.S.P.Q.2d 1445, 1455 (Fed. Cir. 2000) (“In order to satisfy the written description requirement, the disclosure as originally filed need not provide *in haec verba* [‘in these words’] support for the claimed matter at issue.”). Even if the exact phrase “progressive compression” does not appear in the specification, a person of ordinary skill in the art would understand the meaning of this phrase because “progressive compression” is a term that is well-known to a person of ordinary skill in the art. See, for example, the article entitled *Monolithic Logarithmic Amplifiers* submitted with an IDS in Applicant’s response to a prior office action. See also, col. 2, line 22 of U.S. Patent No. 5,805,011.

Claims 2, 10, 19 and 22 are also rejected under 35 U.S.C. §112, first paragraph, as failing to comply with the enablement requirement, and under 35 U.S.C. §112, second paragraph, as being indefinite, based on essentially the same reasoning as the written description requirement. Applicant traverses these rejections. As discussed above, the term “progressive compression” is a term that is well-known to a person of ordinary skill in the art.

Claim Rejections – 35 U.S.C. §102

Claims 2-5, 22-23, 25-27 and 29 are rejected under 35 U.S.C. §102(b) as being anticipated by Yamashita, et al., U.S. Patent No. 4,906,836 (“Yamashita”). Applicant traverses this rejection.

Claim 2 recites that the log amps are progressive compression log amps. Yamashita only discloses log amps that are operational amplifiers configured with feedback diodes for logarithmic operation. Therefore, claim 2 is not anticipated by Yamashita, nor are any claims that depend from claim 2.

Claim 4 recites that the differencing circuit consists essentially of a summing node. In contrast, Yamashita discloses an entire operational amplifier (op amp) circuit identified as AMP1 configured as a differential amplifier rather than a simple summing node. The

Examiner alleges that the positive and negative inputs of AMP1 satisfy the limitation of a summing node. However, the positive and negative inputs of AMP1 are meaningless in the absence of the op amp itself, and thus the claim language “consists essentially of” in claim 4 precludes this interpretation.

Claim 22 recites that logarithmically amplifying comprises progressively compressing. Yamashita does not disclose progressive compression. Instead, Yamashita only discloses the use of simple operational amplifiers configured for logarithmic operation.

Claim 25 recites utilizing a signal to be examined as the first input signal, and utilizing a reference signal as the second input signal. Yamashita does not disclose the use of a reference signal as an input to either of LOG1 and LOG2.

Claim 26 recites that the reference signal has the same waveform as the signal to be examined. The Examiner alleges that claim 26 is anticipated by Yamashita, but does not identify any input signals that have the same waveform.

Claim 27 recites utilizing a modulated signal for the first input signal, and utilizing a modulation signal for the second input signal. Yamashita does not disclose any modulated or modulation signals.

Claim 29 recites that the log amps have current-mode outputs. The output signals e1 and e2 of Yamashita are classic voltage-mode signals output by op amps LOG 1 and LOG 2. The Examiner apparently alleges that the differential voltage between the negative and positive inputs of AMP1 can be considered a current-mode signal. This interpretation, however, is inconsistent with the admitted characterization of the signals at the inputs of AMP1 as voltages.

Thus, claims 2-5, 22-23 and 25-27 and 29 are not anticipated by Yamashita.

Claims 14-15 are rejected under 35 U.S.C. §102(b) as being anticipated by Hashimoto, et al., Japanese Patent No. JP362179635 (“Hashimoto”). Applicant traverses this rejection.

Claims 14 and 15 each recite a differencing circuit. Hashimoto does not disclose a differencing circuit as recited in claims 14 and 15. The Examiner alleges that item 14 shown in Fig. 1 of Hashimoto is a differencing circuit. Item 14, however is an analog-to-digital converter (A/D converter) as explained at page (4), first column, lines 2-3 of Hashimoto. Therefore, claims 14 and 15 are not anticipated by Hashimoto.

Claim Rejections – 35 U.S.C. §103

Claims 6-9, 16-17, 21 and 24 are rejected under 35 U.S.C. §103(a) as being unpatentable over Yamashita in view of Fairley, et al., U.S. Patent No. 5,019,786 (“Fairley”). Applicant traverses this rejection.

Claims 6-9, 16-17 and 21 recite a phase detector core coupled to two log amps. Claim 24 recites multiplying first and second logarithmically amplified signals. The Examiner acknowledges that Yamashita does not disclose a phase detector core, but alleges that it would have been obvious to modify Yamashita to provide the frequency multiplier 30 shown in Fig. 2 of Fairley as a phase detector core. To combine elements from various references, however, there must be some motivation or suggestion to combine the references. Yamashita discloses log amps, but does not provide any suggestion or motivation to couple a phase detector core to them. Fairley discloses a multiplier that might be interpreted as a phase detector core, but does not provide any suggestion or motivation to drive it with two log amps. In essence, the Examiner has reconstructed claim 6, and the other claims rejected under 103(a), by using the claims as a roadmap to piece together selected portions of the prior art without any motivation or teaching to combine those references. This is an impermissible use of hindsight. “One cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention.” *In re Fine*, 5 USPQ2d 1596, 1600 (Fed. Cir. 1988), quoting *W.L. Gore v. Garlock*, 220 USPQ 303, 312-13 (Fed. Cir. 1983). Thus, a *prima facie* case of obviousness has not been established.

Claims 10, 11, 12, 18, 19 and 20 are rejected under 35 U.S.C. §103(a) as being unpatentable over Yamashita. Applicant traverses this rejection.

Claims 10, 19 and 20 recite progressive compression log amps. As discussed above, Yamashita does not disclose progressive compression log amps, and therefore cannot provide a basis for a rejection under Section 103.

Claim 11 recites that the log amps are co-integrated on a substrate and arranged symmetrically about a center line. The Examiner alleges that Yamashita discloses such a center line arrangement, citing a dotted line that has been hand drawn on a copy of Fig. 1 of Yamashita, the dotted line extending horizontally across the entire figure and running directly through the horizontal axis of resistor R3. This drawing is irrelevant, however, because Fig. 1 of Yamashita is merely a schematic diagram that does not provide any geometric layout information. (In contrast, Applicant’s Fig. 6 is expressly described, at page 2, line 3 of the specification, as illustrating the circuit layout.)

Claim 13 is rejected under 35 U.S.C. §103(a) as being unpatentable over Yamashita in view of Barnett, et al., U.S. Patent No. 4,261,056 (“Barnett”). Applicant traverses this rejection.

Claim 13 recites parasitic networks having similar frequency responses. As understood in the art, parasitic circuit elements are unwanted elements that are an unavoidable adjunct of wanted circuit elements. *See The New IEEE Standard Dictionary of Electrical and Electronic Terms* submitted under an IDS with this Response. In one example embodiment disclosed in the specification, for example, at page 7, lines 7-12, parasitic networks may be artifacts of the packaging in which a circuit may be mounted. The Examiner alleges that filters 40, 42, 44 and 41, 43, 45 of Barnett are parasitic networks as recited in claim 13. Barnett’s networks, however, are purpose-made elements fabricated as part of sensor 19, not parasitic elements. Thus, Barnett does not disclose *any* parasitic networks, much less parasitic networks having similar frequency responses as recited in claim 13.

Claim 28 is rejected under 35 U.S.C. §103(a) as being unpatentable over Yamashita in view of Belcher, U.S. Patent No. 5,789,927 (“Belcher”). Applicant traverses this rejection.

Claim 28 recites progressive compression log amps. As discussed above, Yamashita does not disclose progressive compression log amps, and therefore cannot provide a basis for a rejection under Section 103. Moreover, claim 28 also recites two log amps. The Examiner alleges that the hard limiters 21 and 31 illustrated in Fig. 3 of Belcher can be considered log amps. This interpretation, however, is unreasonable in view of the nature of a log amp as providing an output that varies logarithmically in response to the input. In contrast, a hard limiter simply restricts output to some fixed output. *See The New IEEE Standard Dictionary of Electrical and Electronic Terms* submitted under an IDS with this Response.

New Claims

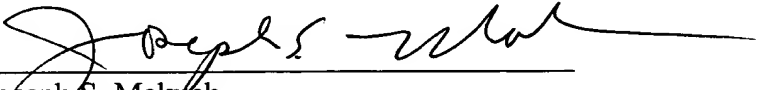
New claims 30 and 31 are added. These claims are derived from claims 2 and 10, respectively, but use the open-ended language “comprise” rather than “are” in defining the characteristics of the log amps.

Conclusion

Applicant requests reconsideration in view of the foregoing amendments and remarks. The Examiner is encouraged to telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

Respectfully submitted,

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